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EXAMINER	
HERNANDEZ, NELSON D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/606,031	MASTER ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernández Hernández	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 49-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 49-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 18, 2008 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on August 8, 2008 is considered by the examiner.

3. The Examiner noted a large number of Non-English documents filed with the IDS with only the abstract being translated to English. MPEP 609.04(a) [R-7] recites: *"The duty of candor does not require that the applicant translate every foreign reference, but only that the applicant refrain from submitting partial translations and concise explanations that it knows will misdirect the examiner's attention from the reference's relevant teaching." 204 F.3d at 1378, 54 USPQ2d at 1008. Although a concise explanation of the relevance of the information is not required for English language information, applicants are encouraged to provide a concise explanation of why the English-language information is being submitted and how it is understood to be*

relevant. Concise explanations (especially those which point out the relevant pages and lines) are helpful to the Office, particularly where documents are lengthy and complex and applicant is aware of a section that is highly relevant to patentability or where a large number of documents are submitted and applicant is aware that one or more are highly relevant to patentability. Therefore, the Examiner only the translated abstract for the Non-English publications is being considered.

4. The Examiner also noted that when considering the documents presented in the IDS, several of the documents are related to liquid dispensing systems, vending machines and devices that do not appear to have any relationship with the present invention. Are those documents mistakenly included in the IDS? If not, please provide an explanation of the relevance of those documents to the present invention. The Examiner considered the documents for Examination purposes. However, the Applicant is advised to provide the correct documents (or document numbers) in the IDS in case other documents were supposed to be present in the IDS.

Claim Objections

5. **Claim 49** is objected to because of the following informalities: in line 11, the limitations "…computational elements each including algorithmic logic, a data input and a data output,, the first …" contain two commas ",,". The limitations should be writes as "…computational elements each including algorithmic logic, a data input and a data output, the first …". Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 7-11, 13-15, 17-26, 49, and 52-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toi, US Patent 7,142,731 in view of DeHon, et al., US Patent 5,956,518.

The Examiner notes that **claims 1, 2, 5-7, 9, 12, 14, 16-19, 49, 51, and 57** are presented using the phrase "**capable of**" in the limitations.

It is noted by the Examiner that the term "**capable of**" is non-limiting and therefore has not been given patentable weight during examination of the claims on their merits. Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. MPEP §2106.

The subject matter of a properly construed claim is defined by the terms that limit its scope. It is this subject matter that must be examined. As a general matter, the grammar and intended meaning of terms used in a claim will dictate whether the language limits the claim scope. Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim:

(A) statements of intended use or field of use,

(B) "adapted to" or "adapted for" clauses,

(C) "wherein" clauses, or

(D) "whereby" clauses.

This list of examples is not intended to be exhaustive. See also MPEP § 2111.04. USPTO personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim should not be read into the claim. E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d 1947, 1950 (Fed. Cir. 2003) (claims must be interpreted "in view of the specification" without importing limitations from the specification into the claims unnecessarily). In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550- 551 (CCPA 1969). See also In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow.... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process.").

Also, it has been held that the recitation that an element is "**capable of**" performing a function is not a positive limitation but only requires the ability to so

perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138.

Regarding claim 1, Toi discloses a digital imaging apparatus (digital camera) comprising:

an optical sensor (solid state image pick-up element 102) capable of converting an object image into a detected image,

an analog-to-digital converter (AD conversions circuit 105) coupled to the optical sensor, the analog-to-digital converter capable of converting the detected image to digital image information (AD conversions circuit 105 are capable of converting the detected image to digital image information),

a plurality of computational units (circuits 400, 401,402, etc.) capable of processing the digital image information to produce a digital image (the plurality of computational units in the FPGA 106 are capable of processing the image information to produce a digital image), the plurality of computational units including a first computational unit having a first architecture of a first plurality of computational elements each including algorithmic logic, a data input and data output (e.g. containing logic for black balance; A computational unit containing logic for black balance, inherently has algorithmic logic, a data input and data output since those elements are necessitated in the circuit to properly perform its operation), and a second computational unit having a second architecture of a second plurality of computational elements each including algorithmic logic, a data input and a data output (e.g.

containing logic for pixel interpolation; A computational unit containing logic for pixel interpolation, inherently has algorithmic logic, a data input and data output since those elements are necessitated in the circuit to properly perform its operation), and

an interconnection network (network that allows the computational elements in field programmable gate array 106 to operate in parallel) coupled to the plurality of computational units (i.e. 400, 401, etc.) and to the A/D converter (105), the interconnection network capable of providing the digital image information to the plurality of computational units, configuring a plurality of computational units for performance of a first imaging function (i.e. color separation processing) on the digital imaging information in response to configuration information that configures the first plurality of computational elements (the interconnection network is capable of configuring a first plurality of computational elements to perform a particular processing (i.e. white balance)) and simultaneously in response to different configuration information to configure the second plurality of computational elements (note that other image computational elements are configured simultaneously with the computational elements forming a computational unit for white balance to perform a different process (i.e. colors space 402, high frequency emphasis 403, and the other arrangements forming different circuits for different processes. See col. 5, line 18 – col. 7, line 15, figs. 4-9)), and reconfiguring the plurality of computational units for performance of a second imaging function (i.e. camera control processing) on the digital image information in response to configuration information (stored in storage device 108) that reconfigures the arrangement of the computational elements in the computational units (note in figs.

4-6 that the interconnection network is capable of reconfiguring the computational units according to the application used in the digital camera; col. 5, line 18 – col. 7, line 15), the first imaging function being different than the second imaging function (the interconnection network is capable of provide the camera with different arrangements for the computational units so that the functions of the computational units are different for each application based on selected applications in the camera; col. 5, line 18 – col. 7, line 15) (Figs. 1 and 4-9, and col. 4, line 12 - col. 7, line 33).

Toi does not explicitly disclose the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; that configuring the plurality of heterogeneous computational units is done by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and that reconfiguring the plurality of computational units is done by reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements.

However, DeHon et al. discloses a reconfigurable integrated circuit (see col. 2, lines 15-20) comprising a plurality of controller elements, the plurality of controller elements including a first controller element and a second controller element (see figs. 1-5, elements F, A, B; col. 5, lines 16-21), the first controller element having a certain architecture and a second controller element having a certain architecture, the first architecture being different from the second architecture (see col. 11, lines 45-49; col. 12, lines 9-12 and 20-25 (description of real-time programmable control architectures);

col. 13, lines 38-40; lines 44-47 (description of a hardwired control architecture); Note the that DeHon discloses two different control schemas are given for control structures. The first (col. 11, lines 45-49; col. 12, lines 9-12 and 20-25) describes a dynamic control system wherein user-defined control structures are selected to be used for implementing a control unit. The second (col. 13, lines 38-40; lines 44-47) describes the use of a hard-wired controlling mechanism which is unable to be defined by a user. Thus, DeHon discloses the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture as claimed); a plurality of dedicated processing elements, the plurality of processing elements including a first processing element and a second processing element (Fig. 4, elements "ALU" etc.), the first processing element having a certain architecture and a second processing element having a certain architecture, the first architecture being different from the second architecture (see col. 2, lines 28-34; lines 43-47; Note that in lines 43-47 De Hon et al. defines an element that is constructed from multiple BFUs which is a different architecture when compared to a BFU that is independent and able to be independently changed. Furthermore, in Fig. 35, DeHon et al. shows a plurality of functional units (elements 512,514, and 516) being hardwired to perform either multiply or add functions, thus defining a rigid architecture. However, in figs. 1-5, DeHon et al. discloses an "ALU" which is routinely configured to perform different operations, similar in spirit to an ALU in a modern processor, which is dynamically configured to perform operations dependent on an instruction being processed. These two different architectures thus define two distinct architectures being utilized within the invention

disclosed by DeHon et al.). DeHon et al. further discloses a reconfigurable interconnection means (see col. 2, lines 6-10; col. 8, lines 18-21), which can be configured by one or a plurality of controller elements, the reconfigurable interconnection means being dynamically reconfigurable in real time (note that in col. 12, lines 7-15, DeHon et al. describes the BFUs reconfiguring each other dynamically, thus in real time), the reconfigurable interconnection means allowing data transfers between processing elements (see DeHon, Fig. 3, connections between ALUs) and data transfers between processing elements and controller elements (see fig. 3, connections between F, A, B, and ALUs], each of said processing element having an output which is connectable to an input of any other said processing element (See fig. 7, connections between BPUs. It is of note that connectable does not necessarily entail that any connection are made) enabling formation of cascaded formation of cascaded function data paths in which parallel operations are performed by each said processing element on data output from a previous processing element in the cascaded data path in a single clock cycle (See fig. 7) (Therefore, the reconfigurable integrated circuit in DeHon et al. teaches that the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; and that is capable of configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units is reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational

elements). DeHon et al. further discloses that by reconfiguring the integrated circuit as described, would allow the computational units to be connected in an application-specific manner so that resources, such as memory and processing, can be deployed in a way that takes advantage of the opportunities for optimization present in any given problem and in addition, configuration memories may be deployed to take advantage of application specific redundancy (Col. 2, lines 4-15).

Therefore, taking the combined teaching of Toi in view of DeHon et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention as made to apply the concept of having a reconfigurable integrated circuit having a plurality of computational units with different architectures and configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units is reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements as taught in DeHon et al. to modify the teaching of Toi to have the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units by reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational

elements. The motivation to do so would have been to allow the computational units to be connected in an application-specific manner so that resources, such as memory and processing, can be deployed in a way that takes advantage of the opportunities for optimization present in any given problem and in addition, configuration memories may be deployed to take advantage of application specific redundancy as suggested by DeHon et al. (Col. 2, lines 4-15).

Regarding claim 7, the limitations of claim 1 are set forth above, and the Toi reference also teaches that the digital imaging apparatus comprises a first memory (RAM 109) couplable to the interconnection network, the first memory capable of storing the processed digital image, as is taught in fig. 1 and col. 4, lines 41-45.

Regarding claim 8, the limitations of claim 7 are taught above by the combined teaching of Toi in view of DeHon et al., and while the combined teaching of Toi does teach a first memory couplable to the interconnection network, Toi fails to specify that the first memory is a selectively removable flash memory. However, Official Notice is hereby taken that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated a removable flash memory device as the first memory of Toi. One would have been motivated to do so because by implementing a removable flash memory, the user could transfer the digitally processed images to external devices without the need of connecting the digital camera to the external device or devices, either wirelessly or through wired connection, as well as

allowing the user to replace memory devices when needed, thereby increasing the portability and ease-of-use of the system.

Regarding claim 9, the limitations of claim 7 are taught above, and Toi also teaches a second memory (EEPROM 108) coupled to the interconnection network, the second memory capable of storing the first configuration information and the second configuration information. See fig. 1 and col. 4, lines 37-65.

Regarding claim 10, the limitations of claim 9 are taught above by the combined teaching of Toi in view of DeHon et al., and while the combined teaching of Toi in view of DeHon al. does not specify that the second memory (108) could be configured as a SDRAM, Official Notice is hereby taken that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented the second memory as an SDRAM. One would have been motivated to do so because it is well known in the art that an SDRAM memory allows instructions to be sent dynamically without waiting for the data to be entirely received, thereby increasing the speed of the transfer of data from the memory to the device.

Regarding claim 11, the limitations of claim 9 are taught above by Toi in view of DeHon et al. Toi further discloses that the first and second memory are EEPROM and SRAM type memories, as is taught in col. 4, lines 19-22 and col. 7, line 7.

Regarding claim 13, the limitations of claim 1 are taught above, and while the combined teaching of Toi in view of DeHon et al. does not specifically disclose that the processed digital image is provided as a plurality of processed digital image packets, it is inherent that the digital processor (FPGA 106) would process the digital image data and provide the digital image data as digital packets, as is well known in the art.

Regarding claim 14, the limitations of claim 13 are set forth above by the combined teaching of Toi in view of DeHon et al., and Toi further discloses a digital output interface (external interface 800) coupled to the interconnection network, wherein the digital output interface outputs a processed digital image (See Fig. 8 and Col. 6, Lines 34-44). What the combined teaching of Toi in view of DeHon et al. does not specifically teach is that the digital output interface is capable of selecting a plurality of digital image data words from the plurality of digital image packets and assembling the plurality of processed digital image data Words to form the processed digital image. However, Official Notice is hereby taken that it would have been well known to one of ordinary skill in the art at the time of the invention to have configured the digital output interface to assemble the plurality of processed digital image data words for output, as assembling digital image data words enables the digital image data to be output without further processing by the external device, thus improving compatibility with various devices.

Regarding claim 15, again the limitations of claim 1 are taught above, and as is similarly shown in claim 13 above, while Toi in view of DeHon et al. does not specifically disclose that the digital image is provided as a plurality of digital image packets, it is inherent that the digital processor (FPGA 106) would process the digital image data and provide the digital image data as digital packets, as is well known in the art.

Regarding claims 17-19, the limitations of claim 1 are taught above by the combined teaching of Toi in view of DeHon et al., and while Toi teaches that the interconnection network is connected to an external device (external equipment 110) in Fig. 8, the combined teaching of Toi in view of DeHon et al. does not specify that the external device connected to the interconnection network is a printer, a dry copier, or a data transmitter. However, Official Notice is hereby taken that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have coupled a printer, a dry copier, or a data transmitter to the interconnection network of Toi, as each of these devices are capable of receiving digital image data and either printing, transferring, or transmitting the processed image on a tangible medium for further manipulation by the user or users.

Regarding claim 20, the limitations of claim 19 are taught above, and Official Notice is also taken that the data transmitter can be any of an analog modem, a digital modem, a DSL modem, or a cable modem, as any of these data transmitters enables

the transfer of image data to a remote location for further viewing, manipulation, or processing, thereby enhancing the portability of the system.

Regarding claim 21, the limitations of claim 1 are taught above, and Toi teaches that the plurality of imaging functions include autofocusing and contrast enhancement, as is taught in figs. 4 and 5, as well as col. 5, line 33 - col. 6, line 6.

Regarding claim 22, again the limitations of claim 1 are set forth above, and Toi in view of DeHon et al. teaches that the algorithmic logic of the first and second plurality of computational elements each perform different functions including functions of configuration, reconfiguration, and field programmability (as inherently present in a field programmable gate array), as is taught in Toi, col. 2, lines 27-36, as well as in col. 4, lines 12 - col. 7, line 33.

Regarding claim 23, the limitations of claim 1 are set forth above, and Toi teaches that the detected image comprises an electrical signal (from solid state image sensor 102) corresponding to the brightness and color variations of the object image, as is taught in col. 4 lines 23-25.

Regarding claim 24, again the limitations of claim 1 are taught above, and Toi discloses that the digital imaging apparatus is embodied as at least one integrated circuit, as shown in fig. 1 and col. 4, lines 12 – col. 7, line 33.

Regarding claim 25, the limitations of claim 1 are shown above, and Toi teaches that the digital imaging apparatus is embodied as a digital camera, as shown in fig. 1.

Regarding claim 26, the limitations of claim 1 are taught above by the combined teaching of Toi in view of DeHon et al., and while Toi only teaches that the digital imaging apparatus is embodied as a digital camera, Official Notice is hereby taken that the digital imaging apparatus could be embodied as either a scanner, a printer, or a dry copier, as the processing circuitry of Toi could easily be configured for use with any type of imaging apparatus, be it a line sensor of a scanner or printer, or an array sensor of a digital camera.

Regarding claim 49, Toi discloses a digital imaging apparatus (digital camera) comprising,

an optical sensor (solid state image pick-up element 102) capable of converting an object image into a detected image,

an analog-to-digital converter (AD conversions circuit 105) coupled to the optical sensor, the analog-to-digital converter capable of converting the detected image to digital image information,

a plurality of computational units (circuits 400, 401,402, etc.), a first computational unit having a first architecture (e.g. containing logic for black balance) of a first plurality of computational elements each including algorithmic logic, a data input and data output (e.g. containing logic for black balance; A computational unit containing

logic for black balance, inherently has algorithmic logic, a data input and data output since those elements are necessitated in the circuit to properly perform its operation), and a second computational element having a second architecture of a second plurality of computational elements each including algorithmic logic, a data input and a data output (e.g. containing logic for pixel interpolation; A computational unit containing logic for pixel interpolation, inherently has algorithmic logic, a data input and data output since those elements are necessitated in the circuit to properly perform its operation), and

an interconnection network (network that allows the computational elements in field programmable gate array 106 to operate in parallel) coupled to the plurality of computational units (i.e. 400, 401, etc.) and to the A/D converter (105), the interconnection network capable of providing a processed digital image from the digital image information, configuring a plurality of computational units for performance of a first imaging function (i.e. color separation processing) in response to configuration information that configures the first plurality of computational elements (the interconnection network is capable of configuring a first plurality of computational elements to perform a particular processing (i.e. white balance), and simultaneously in response to different configuration information to configure the second plurality of computational elements (note that other image computational elements are configured simultaneously with the computational elements forming a computational unit for white balance to perform a different process (i.e. colors space 402, high frequency emphasis 403, and the other arrangements forming different circuits for different processes. See

col. 5, line 18 – col. 7, line 15, figs. 4-9)), and by reconfiguring the plurality of computational units for performance of a second imaging function (i.e. camera control processing) in response to second configuration information (stored in storage device 108) that reconfigures the first plurality of plurality of computational elements in the computational units (note in figs. 4-6 that the interconnection network reconfigures the computational units according to the application used in the digital camera; col. 5, line 18 – col. 7, line 15), the first imaging function being different than the second imaging function (the interconnection network is capable of provide the camera with different arrangements for the computational units so that the functions of the computational units are different for each application based on selected applications in the camera; col. 5, line 18 – col. 7, line 15) (Figs. 1 and 4-9, and col. 4, line 12 - col. 7, line 33) thereby providing a plurality of processed digital image data based on at least the first or second imaging function. Please refer to figs. 1 and 4-8, and col. 4, line 12 – col. 7, line 33. Toi further discloses a digital output interface (external interface 800) coupled to the interconnection network, wherein the digital output interface outputs a processed digital image (See fig. 8 and col. 6, lines 34-44).

Although Toi does not specifically teach is that the digital output interface is capable of selecting a plurality of digital image data words from the plurality of digital image packets and assembling the plurality of processed digital image data words to form the processed digital image. However, Official Notice is hereby taken that it would have been well known to one of ordinary skill in the art at the time of the invention to have configured the digital output interface to assemble the plurality of processed digital

image data words for output, as assembling digital image data words enables the digital image data to be output without further processing by the external device, thus improving compatibility with various devices.

Toi does not explicitly disclose the computational elements as heterogeneous computational elements and that the first fixed architecture is different from the second fixed architecture; that configuring the plurality of heterogeneous computational elements is done by configuring the interconnections in the interconnection network between at least the first and second computational elements; and that reconfiguring the plurality of computational elements is done by reconfiguring the interconnections in the interconnection network between at least the first and second computational elements.

However, DeHon et al. discloses a reconfigurable integrated circuit (see col. 2, lines 15-20) comprising a plurality of controller elements, the plurality of controller elements including a first controller element and a second controller element (see figs. 1-5, elements F, A, B; col. 5, lines 16-21), the first controller element having a certain architecture and a second controller element having a certain architecture, the first architecture being different from the second architecture (see col. 11, lines 45-49; col. 12, lines 9-12 and 20-25 (description of real-time programmable control architectures); col. 13, lines 38-40; lines 44-47 (description of a hardwired control architecture); Note the that DeHon discloses two different control schemas are given for control structures. The first (col. 11, lines 45-49; col. 12, lines 9-12 and 20-25) describes a dynamic control system wherein user-defined control structures are selected to be used for

implementing a control unit. The second (col. 13, lines 38-40; lines 44-47) describes the use of a hard-wired controlling mechanism which is unable to be defined by a user. Thus, DeHon discloses the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture as claimed); a plurality of dedicated processing elements, the plurality of processing elements including a first processing element and a second processing element (Fig. 4, elements "ALU" etc.), the first processing element having a certain architecture and a second processing element having a certain architecture, the first architecture being different from the second architecture (see col. 2, lines 28-34; lines 43-47; Note that in lines 43-47 De Hon et al. defines an element that is constructed from multiple BFUs which is a different architecture when compared to a BFU that is independent and able to be independently changed. Furthermore, in Fig. 35, DeHon et al. shows a plurality of functional units (elements 512,514, and 516) being hardwired to perform either multiply or add functions, thus defining a rigid architecture. However, in figs. 1-5, DeHon et al. discloses an "ALU" which is routinely configured to perform different operations, similar in spirit to an ALU in a modern processor, which is dynamically configured to perform operations dependent on an instruction being processed. These two different architectures thus define two distinct architectures being utilized within the invention disclosed by DeHon et al.). DeHon et al. further discloses a reconfigurable interconnection means (see col. 2, lines 6-10; col. 8, lines 18-21), which can be configured by one or a plurality of controller elements, the reconfigurable interconnection means being dynamically reconfigurable in real time (note that in col.

12, lines 7-15, DeHon et al. describes the BFUs reconfiguring each other dynamically, thus in real time), the reconfigurable interconnection means allowing data transfers between processing elements (see DeHon, Fig. 3, connections between ALUs) and data transfers between processing elements and controller elements (see fig. 3, connections between F, A, B, and ALUs], each of said processing element having an output which is connectable to an input of any other said processing element (See fig. 7, connections between BPUs. It is of note that connectable does not necessarily entail that any connection are made) enabling formation of cascaded formation of cascaded function data paths in which parallel operations are performed by each said processing element on data output from a previous processing element in the cascaded data path in a single clock cycle (See fig. 7) (Therefore, the reconfigurable integrated circuit in DeHon et al. teaches that the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; and that is capable of configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units is reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements). DeHon et al. further discloses that by reconfiguring the integrated circuit as described, would allow the computational units to be connected in an application-specific manner so that resources, such as memory and processing, can be deployed in a way that takes advantage of the opportunities for optimization present in any given

problem and in addition, configuration memories may be deployed to take advantage of application specific redundancy (Col. 2, lines 4-15).

Therefore, taking the combined teaching of Toi in view of DeHon et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention as made to apply the concept of having a reconfigurable integrated circuit having a plurality of computational units with different architectures and configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units is reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements as taught in DeHon et al. to modify the teaching of Toi to have the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units by reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements. The motivation to do so would have been to allow the computational units to be connected in an application-specific manner so that resources, such as memory and processing, can be deployed in a way that takes advantage of the opportunities for optimization present in any given problem and in addition, configuration memories may

be deployed to take advantage of application specific redundancy as suggested by DeHon et al. (Col. 2, lines 4-15).

Regarding claim 52, the limitations of claim 49 are set forth above, and Toi further discloses that the plurality of imaging functions include autofocusing and contrast enhancement, as is taught in figs. 4 and 5, as well as col. 5, line 33 - col. 6, line 6.

Regarding claim 53, again the limitations of claim 49 are set forth above, and Toi discloses that that the algorithmic logic of the first and second plurality of computational elements each perform different functions including functions of configuration, reconfiguration, and field programmability (as inherently present in a field programmable gate array), as is taught in Col. 2, Lines 27-36, as well as in Col. 4, Lines 12 -Col. 7, Line 33.

Regarding claim 54, the limitations of claim 49 are set forth above, and Toi teaches that the digital imaging apparatus is embodied as a digital camera, as shown in fig. 1.

Regarding claim 55, claim 55 is a method claim of the apparatus in claims 1 and 49. Therefore, limitations have been discussed and analyzed in claims 1 and 49.

Regarding claim 56, Toi discloses a digital imaging apparatus (digital camera), comprising:

a digital image information input (output AD conversions circuit 105);

a plurality of computational units (circuits 400, 401,402, etc.) to process digital image information to produce a processed digital image, the plurality of computational units including a first computational unit having a first architecture (e.g. containing logic for black balance) of a first plurality of computational elements each including algorithmic logic, a data input and a data output (e.g. containing logic for black balance; A computational unit containing logic for black balance, inherently has algorithmic logic, a data input and data output since those elements are necessitated in the circuit to properly perform its operation), and a second computational unit having a second architecture of a second plurality of computational elements each including algorithmic logic, a data input and a data output (e.g. containing logic for pixel interpolation; A computational unit containing logic for pixel interpolation, inherently has algorithmic logic, a data input and data output since those elements are necessitated in the circuit to properly perform its operation; and

an interconnection network (network that allows the computational elements in field programmable gate array 106 to operate in parallel) coupled to the plurality of computational units, the interconnection network providing the digital image information to the plurality of computational elements and configuring the plurality of computational units to perform a first imaging function (i.e. color separation processing; the interconnection network configures a first plurality of computational elements to perform

a particular processing (i.e. white balance)) by simultaneous providing different configuration information to configure the first plurality of computational elements and the second plurality of computational elements (note that other image computational elements are configured simultaneously with the computational elements forming a computational unit for white balance to perform a different process (i.e. colors space 402, high frequency emphasis 403, and the other arrangements forming different circuits for different processes. See col. 5, line 18 – col. 7, line 15, figs. 4-9)), and reconfiguring the plurality of computational units for performance of a second imaging function (i.e. camera control processing) in response to providing configuration information that reconfigures at least some of the first plurality of computational elements (note in figs. 4-6 that the interconnection network reconfigures the computational units according to the application used in the digital camera; col. 5, line 18 – col. 7, line 15), the first imaging function being different than the second imaging function (the interconnection network is capable of provide the camera with different arrangements for the computational units so that the functions of the computational units are different for each application based on selected applications in the camera; col. 5, line 18 – col. 7, line 15) (Figs. 1 and 4-9, and col. 4, line 12 - col. 7, line 33) (See also figs. 1 and 4-8, and col. 4, line 12 – col. 7, line 33).

Toi does not explicitly disclose the computational elements as heterogeneous computational elements and that the first fixed architecture is different from the second fixed architecture; that configuring the plurality of heterogeneous computational elements is done by configuring the interconnections in the interconnection network

between at least the first and second computational elements; and that reconfiguring the plurality of computational elements is done by reconfiguring the interconnections in the interconnection network between at least the first and second computational elements.

However, DeHon et al. discloses a reconfigurable integrated circuit (see col. 2, lines 15-20) comprising a plurality of controller elements, the plurality of controller elements including a first controller element and a second controller element (see figs. 1-5, elements F, A, B; col. 5, lines 16-21), the first controller element having a certain architecture and a second controller element having a certain architecture, the first architecture being different from the second architecture (see col. 11, lines 45-49; col. 12, lines 9-12 and 20-25 (description of real-time programmable control architectures); col. 13, lines 38-40; lines 44-47 (description of a hardwired control architecture); Note the that DeHon discloses two different control schemas are given for control structures. The first (col. 11, lines 45-49; col. 12, lines 9-12 and 20-25) describes a dynamic control system wherein user-defined control structures are selected to be used for implementing a control unit. The second (col. 13, lines 38-40; lines 44-47) describes the use of a hard-wired controlling mechanism which is unable to be defined by a user. Thus, DeHon discloses the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture as claimed); a plurality of dedicated processing elements, the plurality of processing elements including a first processing element and a second processing element (Fig. 4, elements "ALU" etc.), the first processing element having a certain architecture and a

second processing element having a certain architecture, the first architecture being different from the second architecture (see col. 2, lines 28-34; lines 43-47; Note that in lines 43-47 De Hon et al. defines an element that is constructed from multiple BFUs which is a different architecture when compared to a BFU that is independent and able to be independently changed. Furthermore, in Fig. 35, DeHon et al. shows a plurality of functional units (elements 512,514, and 516) being hardwired to perform either multiply or add functions, thus defining a rigid architecture. However, in figs. 1-5, DeHon et al. discloses an "ALU" which is routinely configured to perform different operations, similar in spirit to an ALU in a modern processor, which is dynamically configured to perform operations dependent on an instruction being processed. These two different architectures thus define two distinct architectures being utilized within the invention disclosed by DeHon et al.). DeHon et al. further discloses a reconfigurable interconnection means (see col. 2, lines 6-10; col. 8, lines 18-21), which can be configured by one or a plurality of controller elements, the reconfigurable interconnection means being dynamically reconfigurable in real time (note that in col. 12, lines 7-15, DeHon et al. describes the BFUs reconfiguring each other dynamically, thus in real time), the reconfigurable interconnection means allowing data transfers between processing elements (see DeHon, Fig. 3, connections between ALUs) and data transfers between processing elements and controller elements (see fig. 3, connections between F, A, B, and ALUs], each of said processing element having an output which is connectable to an input of any other said processing element (See fig. 7, connections between BPUs. It is of note that connectable does not necessarily entail

that any connection are made) enabling formation of cascaded formation of cascaded function data paths in which parallel operations are performed by each said processing element on data output from a previous processing element in the cascaded data path in a single clock cycle (See fig. 7) (Therefore, the reconfigurable integrated circuit in DeHon et al. teaches that the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; and that configures the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units is reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements). DeHon et al. further discloses that by reconfiguring the integrated circuit as described, would allow the computational units to be connected in an application-specific manner so that resources, such as memory and processing, can be deployed in a way that takes advantage of the opportunities for optimization present in any given problem and in addition, configuration memories may be deployed to take advantage of application specific redundancy (Col. 2, lines 4-15).

Therefore, taking the combined teaching of Toi in view of DeHon et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention as made to apply the concept of having a reconfigurable integrated circuit having a plurality of computational units with different architectures and configuring the plurality of heterogeneous computational units by configuring the interconnections in the

interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units is reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements as taught in DeHon et al. to modify the teaching of Toi to have the computational elements as heterogeneous computational units and that the first fixed architecture is different from the second fixed architecture; configuring the plurality of heterogeneous computational units by configuring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements; and reconfiguring the plurality of computational units by reconfiguring the interconnections in the interconnection network between at least the first plurality and second plurality of computational elements. The motivation to do so would have been to allow the computational units to be connected in an application-specific manner so that resources, such as memory and processing, can be deployed in a way that takes advantage of the opportunities for optimization present in any given problem and in addition, configuration memories may be deployed to take advantage of application specific redundancy as suggested by DeHon et al. (Col. 2, lines 4-15).

Regarding claim 57, the limitations of claim 56 are set forth above, and Toi teaches an optical sensor (solid state image pick-up element 102) capable of converting an object image into a detected image; and an analog-to-digital converter (AD conversions circuit 105) coupled to the optical sensor, the analog-to-digital converter

capable of converting the detected image to the digital image information, the converter coupled to the digital image input (See Toi, col. 4, lines 12-45).

8. Claims 2-6, 12, and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toi (U.S. Pat. 7,142,731) in view of DeHon, et al., US Patent 5,956,518 and further in view of Deng et al. (U.S. Pat. 6,778,212).

Regarding claim 2, the limitations of claim 1 are set forth above, and while Toi does teach that the lens system (100) is controlled by control circuit 101, the combined teaching of Toi in view of DeHon et al. fails to specifically disclose that the digital imaging apparatus comprises a focusing means capable of providing the object to the optical sensor. However, noting the Deng reference, Deng teaches a focusing means (motor 22 for adjusting focus of lens 21) capable of providing the object image to the optical sensor (image sensor 100). Please refer to Fig. 5 and Col. 7, Lines 38-41. It would have been obvious to one of ordinary skill in the art to have included the focusing means of Deng with the digital imaging apparatus of Toi and DeHon et al., as by providing a focusing means, the image obtained by the imaging apparatus will be of much higher quality in situations where a fixed-focus lens cannot provide the optimal in-focus resolution.

Regarding claim 3, the limitations of claim 2 are set forth above, and Deng further teaches that the focusing means comprises a focusing assembly, the focusing

assembly further comprising a lens (21), as shutter, an aperture, and a focusing motor (22), as is again taught in fig. 5 and col. 7, lines 38-41.

Regarding claim 4, the limitations of claim 1 are taught above by the combined teaching of Toi in view of DeHon et al., and while Toi does teach the optical sensor (solid state image pick-up element 102), Toi does not specify the type of optical sensor employed. However, the Deng reference teaches an optical sensor (100) that is a CMOS array, as taught in col. 3, lines 44-56.

Regarding claim 5, again the limitations of claim 1 are taught above by the combined teaching of Toi in view of DeHon et al., and while Toi does teach that a viewfinder screen (display device. 107) is coupled to the FPGA 106, Toi does not specifically teach an analog output interface coupled to the interconnection network, the analog output interface capable of converting the processed digital image into an analog form, and a viewfinder screen coupled to the analog output interface, the viewfinder screen capable of visually displaying the analog form of the processed digital image. However, Deng teaches in an analog output interface (FPGA 18 coupled to video port 23) coupled to the interconnection network (of FPGA 18), the analog output interface inherently capable of converting the processed digital image to an analog form, and a viewfinder screen (LCD panel 24 and/or TV display 25) coupled to the analog output interface, the viewfinder screen capable of visually displaying the analog form of the processed digital image. Please refer to fig. 5 and col. 7, lines 34-48.

Regarding claim 6, again the limitations of claim 1 are shown above, and Deng teaches in an analog output interface (FPGA 18 coupled to video port 23) coupled to the interconnection network (of FPGA 18), the analog output interface inherently capable of converting the processed digital image to an analog form, and an analog output port (video port 23) coupled to the analog output interface, the analog output port capable of outputting the analog form of the processed digital image. Please refer to fig. 5 and col. 7, lines 34-48.

Regarding claim 12, the limitations of claim 1 are set forth above, and while Toi does show that digital image information can be sent to external equipment via external interface 800 (See Fig. 8), the combined teaching of Toi in view of DeHon et al. fails to specifically show a digital output port coupled to the interconnection network, the digital output port capable of outputting the processed digital image. However, the Deng reference teaches a digital output port (com port 26) coupled to the interconnection network, the digital output port capable of outputting the processed digital image. Please refer to fig. 5 and col. 7, lines 34-48.

Regarding claim 50, the limitations of claim 49 are taught above, and while Toi does teach the optical sensor (solid state image pick-up element 102), the combined teaching of Toi in view of DeHon et al. does not specify the type of optical sensor

employed. However, the Deng reference teaches an optical sensor (100) that is a CMOS array, as taught in col. 3, lines 44-56.

Regarding claim 51, again the limitations of claim 49 are set forth above, and the Deng reference teaches analog output interface (FPGA 18 coupled to video port 23) coupled to the interconnection network (of FPGA 18), the analog output interface inherently capable of converting the processed digital image to an analog form, and a viewfinder screen (LCD panel 24 and/or TV display 25) coupled to the analog output interface, the viewfinder screen capable of visually displaying the analog form of the processed digital image. Deng further shows an analog output port (video port 23) coupled to the analog output interface, the analog output port capable of outputting the analog form of the processed digital image, and a digital output port (corn port 26) coupled to the interconnection network, the digital output port capable of outputting the processed digital image. Please refer to Fig. 5 and Col. 7, Lines 34-48.

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toi US Patent 7,142,731 in view of DeHon, et al., US Patent 5,956,518 and further in view of Fukuoka, US Patent 5,754,227.

Regarding claim 16, the limitations of claim 1 are taught above by the combined teaching of Toi in view of DeHon et al., but Toi fails to specifically disclose that the imaging apparatus further comprises a light source capable of providing light for reflection from an object to form the object image.

However, the Fukuoka reference teaches a digital imaging apparatus (digital camera 30) comprising a light source (flash :20) capable of providing light for reflection from an object to form the object image (See Fig. 6 and col. 4, line 54 - col. 5, line 67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the light source of Fukuoka with the digital imaging apparatus of Toi and DeHon et al. One would have been motivated to do so because the use of a light source allows suitable images to be captured in low ambient light conditions, such as indoors, and thus allows the digital imaging apparatus to be used effectively in a variety of locations.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernández Hernández whose telephone number is (571)272-7311. The examiner can normally be reached on 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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